An Embedded Planar-Foil Capacitor Material, FPGA Based Interposer, Aimed at Improving System Performance and Reduced Board Size for Space Based Electronics

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Abstract— This paper presents work to date in developing, and testing an embedded planar-foil capacitor based interposer intended to be integrated together with high-density components such as Field Programmable Gate Arrays (FPGAs), and Application Specific Integrated Circuits (ASIC). FPGA devices typically have a large number of I/O and power pins. The high speed enabled by these devices requires a large number of discrete bypass capacitors as close as possible to the power pins. These capacitors take up a considerable amount of the board area on the application circuit board. The developed interposer replaces these components freeing up space of traditional bypass capacitors for other circuitry.

The Interposer was developed based on the requirements of Microsemi's RTG4 FPGA. The interposer was developed using COTS embedded foil capacitors. The Interposer is customized to the capacitance requirements for each of the FPGA banks. Three foil manufactures were evaluated: Oak Mitsui, 3M and TDK. Out of the three different manufactures designs that were evaluated, the Oak-Mitsui based Interposer was the one constructed and tested. Through simulations, the horizontal and vertical interconnect inductances were validated and the FPGA decoupling requirements were shown to be met. The use of the interposer results in an overall reduction in Printed Wiring Board (PWB) area.

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1. Introduction

This work is part of the JPL/NASA Europa Lander's Technology Maturation Effort, focused on a miniaturized next generation Motor Control. The goal is to allow a potential Europa Lander to last longer on the surface or allow more room for additional science instruments by reducing the volume, mass and power of motor control avionics and the amount of energy required to keep the avionics warm.

The mass requirement is addressed by developing modular standardized Multi-Chip Modules (MCMs), utilizing advanced substrate and System-in-Package (SiP) technologies that can be configured into a compact yet versatile avionics topology that significantly reduces Size, Weight, and Power (SWaP) over previously flown avionics assemblies.

The focus of our planar-foil based capacitor interposer and integrated FPGA topology follows the SiP theme, by developing a standardized integrated solution resulting in an overall reduction in our Printed Wiring Board (PWB) area. We will show how this freed space traditionally used for bypass capacitors will be leveraged when developing highly integrated avionics solution.

2. Architecture

Typical components of a circuit board's power distribution system include a switching power supply, inner layer power and ground planes, bulk decoupling and high frequency decoupling capacitors.

When using an FPGA based design, specific power supply filtering techniques are needed, along with supplemental good board layout practices to achieve low noise levels, signal integrity, impedance and general power conditioning.

To achieve reduced fluctuations on the power supply lines, FPGA devices require a large number of discrete bypass capacitors as close as possible to the power

pins. Table 1 represents the number of bypass capacitor required for a typical application of the Microsemi FPGA.

Power Supply Decoupling Capacitors for CG1657

External on Board Capacitors				External on Board Capacitors			
Pin Name	Number of Pins	0.01 uF	0.1 uF	Pin Name	Number of Pins	0.01 uF	0.1 uF
VDDI4	15	7	7	SERDES_3_L01_VDDA	6	0	6
VDDI5	16	8	8	SERDES_3_L23_VDDA	6	0	6
VDDI6	15	8	8	SERDES_4_L01_VDDA	6	0	6
VDDI7	16	8	8	SERDES_4_L23_VDDA	6	0	6
VDDI8	16	8	8	SERDES_PCIE_5_L01_VDDAIO	6	0	6
VDDI9	20	10	10	SERDES_P_CIE_5_L23_VDDAIO	6	0	6
VDDPLL	13	13	13	SERDES_P_CIE_0_L01_VDDAPLL	1	0	1
VPP	9	9	9	SERDES_P_CIE_0_L23_VDDAPLL	1	0	1
VREF0	2	2	2	SERDES_1_L01_VDDA_PLL	1	0	1
VREF9	2	2	2	SERDES_1_L23_VDDA_PLL	1	0	1
SERDES_V DDI	4	2	2	SERDES_2_L01_VDDA_PLL	1	0	1
SERDES_V REF	2	0	2	SERDES_2_L23_VDDA_PLL	1	0	1
SERDES_P / CIE_0_L01_VDDAIO	6	0	6	SERDES_3_L01_VDDA_PLL	1	0	1
SERDES_P / CIE_0_L23_VDDAIO	6	0	6	SERDES_3_L23_VDDA_PLL	1	0	1
SERDES_1_L01_VDDA	6	0	6	SERDES_4_L01_VDDA_PLL	1	0	1
SERDES_1_L23_VDDA	6	0	6	SERDES_4_L23_VDDA_PLL	1	0	1
SERDES_2_L01_VDDA	6	0	6	SERDES_P_CIE_5_L01_VDDAPLL	1	0	1
SERDES_2_L23_VDDA	6	0	6	SERDES_P_CIE_5_L23__VDDAPLL	1	0	1

Table 1. *Typical large number of bypass capacitors required to meet power-conditioning guidelines.*

The large number of capacitors (qty: 125 of 0.01uF and qty: 163 of 0.1uF) are placed on the top and or bottom of the printed wiring assembly (PWA), generally directly behind the FPGA. Figure 1 represents the pathfinder Europa Lander Sphinx computer showing FPGA/bypass capacitor placement, requiring a large area of the backside of the PWA under the FPGA to meet power-conditioning guidelines.

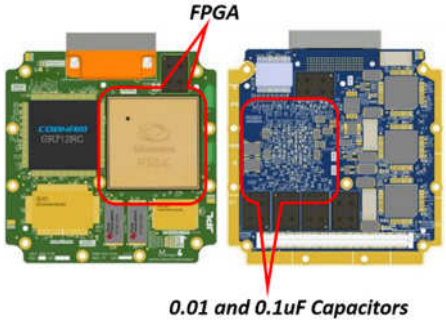


Figure 1. *Typical SoP implementation of FPGA and bypass capacitors, requiring usage of large area of the PWA.*

This packaging topology is typical, mass and volume reduction is difficult to achieve. Illustration of the SoP architecture is depicted in Figure 2a. Alternately, placing capacitive foil based “Interposer” directly under the FPGA provides customized capacitance to the FPGA power banks, resulting in improved horizontal and vertical interconnect inductances, but most importantly the ability to use the PWA area typically used for bypass capacitors can now be used for additional circuit functions. Figure 2b illustration represents the use of SoA COTS planar-foil technology.

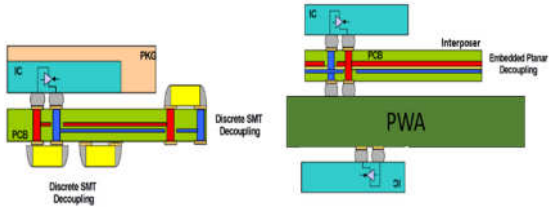


Figure 2a. *Represents SoP use of bypass capacitors directly under or alongside the FPGA,* ***Figure 2b****. Represents SoA using COTS planar-foil technology between the FPGA and PWA, allowing more function to be place behind the FPGA.*

3. Key Technology Development

The goal for the Interposer design was to implement a SiP themed solution between the FPGA and PWA, requiring a construction suitable of foil capacitor technology and driven by need to leverage PWB area used for the Bypass Capacitors shown in figure 1, miniaturization, performance and component reduction.

The use of planer-foil capacitors technology systems are not new to the industry. A few hundred nanofarads of embedded low inductance capacitance can eliminate large number of surface mount decoupling capacitors in a typical power-ground core based printed wiring board assembly [1][2].

Literature search revealed many different planar-foils technologies. Three foil manufactures were evaluated: Oak-Mitsui – FaradFlex Technology [3], 3M – Embedded Capacitance Material (ECM) Technology [4] and TDK – Ferroelectric foil Technology [5].

Impedances where calculated for the Motor Control design based on the Microsemi RTG4 specification for the worst-case power voltages and performance at 24 MHz, are shown in table 2. These targeted impedances help determine the number of capacitive layers needed in the Interposer PWB stackup to meet system requirements.

Nominal Dissipation

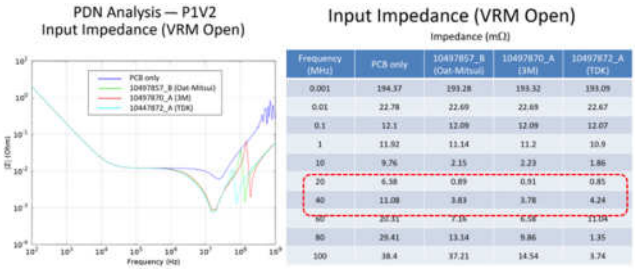
Name	min(V)	nom(V)	max (V)	Allowable Ripple (%)	Desired Ripple (%)	Supply Current (A)	Target Impedance(Ω)
P1V2	1.14	1.2	1.26	5%	5%	0.7	85.7E-3
P2V5	2.375	2.5	2.625	5%	5%	0.1	1.25
P3V3	3.15	3.3	3.45	5%	5%	0.2	750.0E-3
VDDMEM	2.375	2.5	2.625	5%	5%	0.1	1.25
VDDB12	2.375	2.5	2.625	5%	5%	0.1	1.25
VDDB78	2.375	2.5	2.625	5%	5%	0.1	1.25
P3V3A_PLL	3.15	3.3	3.45	5%	5%	0.01	15

Maximum Dissipation

Name	min(V)	nom(V)	max (V)	Allowable Ripple (%)	Desired Ripple (%)	Supply Current (A)	Target Impedance(Ω)
P1V2	1.14	1.2	1.26	5%	5%	1.34	44.8E-3
P2V5	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
P3V3	3.15	3.3	3.45	5%	5%	1	150.0E-3
VDDMEM	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
VDDB12	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
VDDB78	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
P3V3A_PLL	3.15	3.3	3.45	5%	5%	0.01	15

Table 2. *Motor control system impedances where calculated based on the RTG4 specification for the worst-case power voltages and allowable performance at 24 MHz*

Preliminary Interposer PWB stack-up configurations were provided to Aurora Systems to perform Power Distribution Network (PDM) analysis. Results shown in figure 3, represent the worst-case power bank voltage for the 1.2V solution for all three candidate planar-foils. System impedances (mΩ) requirements at a given frequency (MHz) have been met for the motor control FPGA performance.



Frequency (MHz)	PCB only	10497857_B (Oat-Mitsui)	10497870_A (3M)	10497872_A (TDK)
0.001	194.37	193.28	193.32	193.09
0.01	22.78	22.69	22.69	22.67
0.1	12.1	12.09	12.09	12.07
1	11.92	11.14	11.2	10.9
10	9.76	2.15	2.23	1.86
20	6.58	0.89	0.91	0.85
40	11.09	3.83	3.78	4.24
60	17.51	7.05	6.56	11.04
80	29.41	13.14	9.86	1.35
100	38.4	37.21	14.54	3.74

Figure 3. *Power Density Analysis results, representative of the 1.2V FPGA power pin impedance, analytically showing foil performance for all three capacitive technologies meet motor control performance.*

4. PWB Design and Manufacturing

Leveraging the results of the PDM analysis, a multi plane stackup was created using four foil layers for the 1.2V plane and one each foil plane layer(s) for the balance of the power-bank voltages. Oak-Mitsui planar-foil technology was selected based on previous test build experiences.

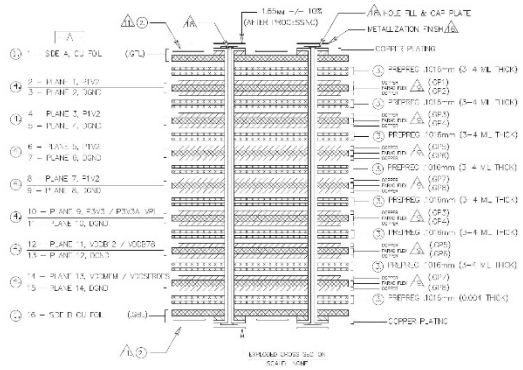


Figure 4. *Interposer PWB Stackup, 16 layers with seven capacitive planar-foil layers and 2 copper outer layers. Built using standard multi-layer processing.*

PWB construction processing was typical multi-layer construction, 8-mil drill for vias with via-in pad design, CB100 hole-fill, Cu-wrap-plate and capped construction. PWB finish metallization is ENEPIG (electroless nickel / electroless palladium / immersion gold) per IPC-4556. Figures 5f and 7 show the completed Interposer PWB.

As an alternate build option and based on the established PWB design, additional 0.1uF – 0201 capacitors were used to meet the specific decoupling requirements of future RTG4 applications based on the Microsemi RTG4 board design guidelines. Figure 5 shows the new PWB design layout showing how the discrete capacitors are connected to a specific voltage power-bank. This solution improved total capacitance capability.

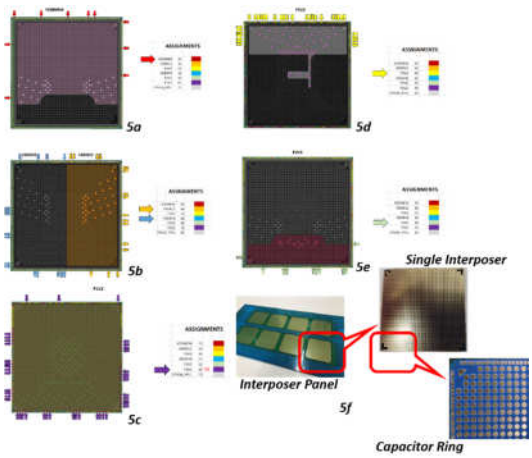


Figure 5a-5e. *Represent each of the 5-voltage internal planes, color-coded represents new discrete capacitor, associated locations and count.* ***Figure 5f.*** *Shows the completed Interposer PWB and a close up of the ring of capacitors along the edge of the substrate.*

Careertech-US was selected to fabricate all three of the planar-foil technologies. Oak-Mitsui construction is represented in figures 4 and 5 and currently baselined for all future Motor Control Electronics planned for near term missions. The Oak-Mitsui product did not require special processing and no manufacturing issues came to light during fabrication.

5. System Integration

The goal of this Interposer/FPGA SiP solution required a direct infusion into the Europa Lander's Motor Control PWA topology. This infusion needed to be a repeatable application for any PWA incorporating an FPGA based electronic design. Figure 6 represents the current Pathfinder Motor Control Assembly with the Interposer/FPGA integrated. The Interposer/FPGA does not take up any additional volume on the top side of the PWA, and the area directly under the FPGA or backside of the PWA was used for additional components / functions.

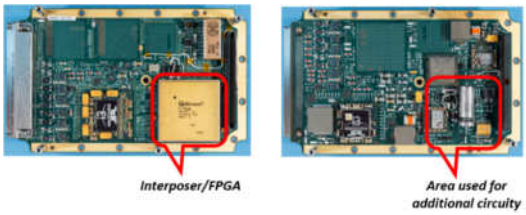


Figure 6. *New Capacitive foil based Interposer/FPGA SiP Assembly attachment within the Europa Lander Motor Controller.*

Figure 7 shows a close up view of the Interposer/FPGA assembly attached to the Motor Control Assembly. The processing sequence is as follows Interposer: screen-place-eutectic reflow of solder spheres, followed by screen-place-eutectic reflow of Interposer PWB and FPGA device, followed by screen-place-eutectic reflow of Interposer/FPGA to Motor Control PWA. Each sequence included a DI wash, two-hour bake @ 125C and inspection. X-ray results indicated no processing issues.

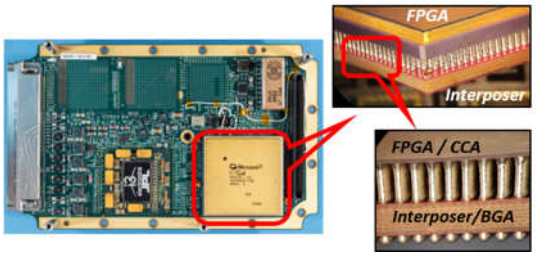


Figure 7. *Capacitive foil based Interposer and Microsemi FPGA integrated onto the Motor Control Assembly*

6. Validation

To validate the Interposer performance, we compared the predicted capacitance for each power plane with measured values for the Oak-Mitsui PWBs. Table 3 shows measured vs predicted results.

Measurements Vs Predicted							
Plane	Plus	Minus	Measured Resistance.	Predicted Capacitance	Measured Capacitance		%Error
VDDMEM	AN40	AW2	OPEN	47.75879572	49	nF	3%
VDDB12	C40	AW2	OPEN	32.15340048	29	nF	10%
P3V3	A36	AW2	OPEN	22.3083605	20	nF	10%
VDDB78	C2	AW2	OPEN	32.15340048	29	nF	10%
VDDMEM	AM9	AW2	OPEN	47.75879572	45	nF	6%
P2V5	AN21	AW2	OPEN	16.54800523	14	nF	15%
P1V2	N15	AW2	OPEN	257.2272038	239	nF	7%
P3V3A_VPLL	N21	AW2	OPEN	41.99844045	38	nF	10%

Table 3. *Predicted Vs Measured Capacitance Density measurements of the fabricated Interposer PWB.*

7. Conclusion

This effort demonstrated design, fabrication, assembly and testing of a planar-foil Interposer/FPGA SiP technology, which met the goals of improved functionality and demonstrated overall reduction in Printed Wiring Board (PWB) area over present state of practice. Future functional tests of the Europa Lander Motor Control Assembly will provide confidence that the Interposer/FPGA SiP is ready to be incorporated into future designs.

8. Acknowledgements

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