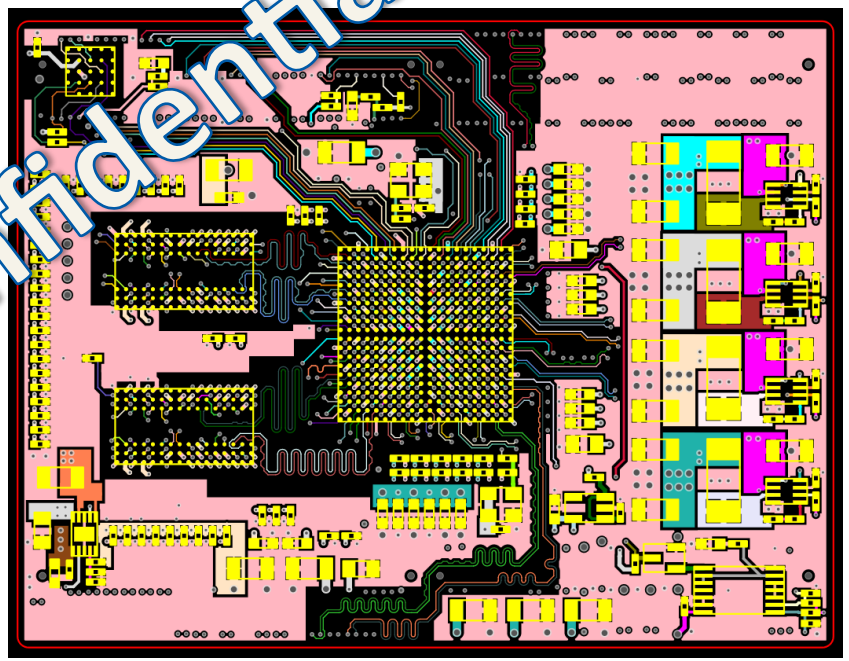
PDN Analysis Report

xxx xxx 2017

Design Summary

Design Information	
Name	test
Layout Format	Allegro
Board Size	xxx
Total # of Components	xxx
Metal Layers	10
Core Power Information	
Core Power Net	VCC_3.3
Voltage	3.3V
SoC component	Xxx:xxx
VRM component	xxx: U2
Number of Decaps	30



Stackup Information

Type	Name	Thickness (mil)	Dielectric Constant	Loss Tangent
Metal	TOP	1.4		
Dielectric	LD_TOP	5.9	4.2	0.02
Metal	GND1	1.4		
Dielectric	LD_GND1	5.1	4.2	0.02
Metal	SIG1	1.4		
Dielectric	LD_SIG1	4.5	4.2	0.02
Metal	SIG2	1.4		
Dielectric	LD_SIG2	5.1	4.2	0.02
Metal	POWER1	1.4		
Metal	POWER2	1.4		
Dielectric	LD_POWER2	5.1	4.2	0.02
Metal	SIG3	1.4		
Dielectric	[illegible]	4.5	4.2	0.02
Metal	[illegible]G4	1.4		
Dielectric	LD_SIG4	5.1	4.2	0.02
Metal	GND2	1.4		
Dielectric	LD_GND2	5.9	4.2	0.02
Metal	BOTTOM	1.4		

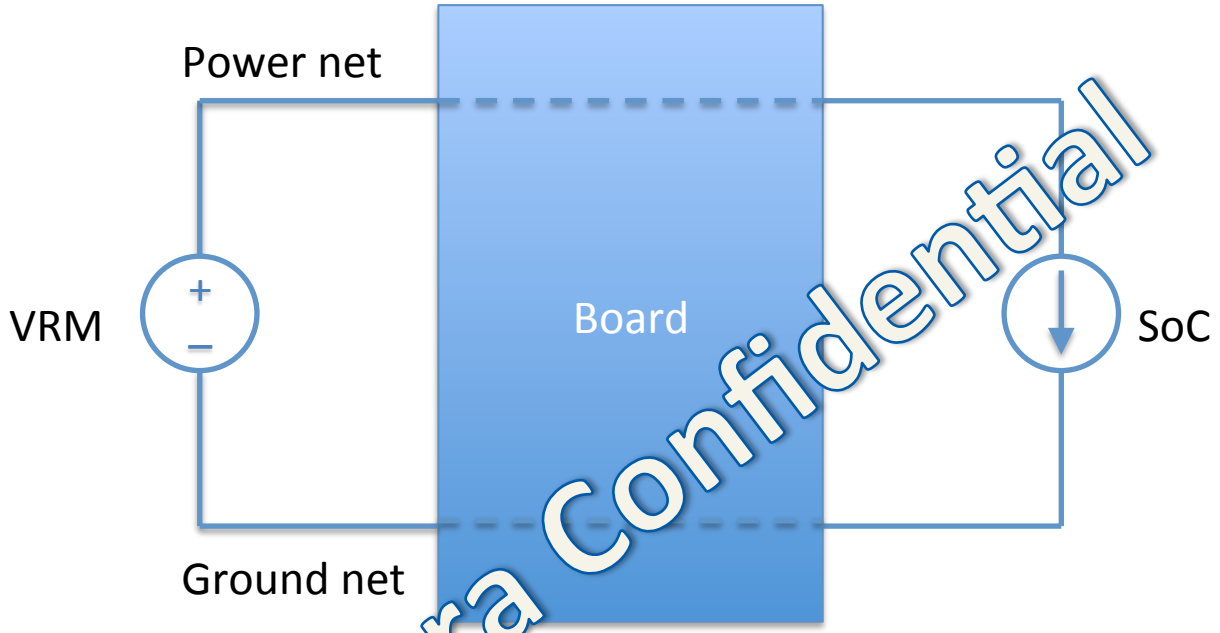
Service Summary

Service Performed	Service Scope	Report
DC Voltage Drop	VCC_3V3, GND	DC Voltage distribution plot
AC Impedance	VCC_3V3, GND	Frequency domain impedance Plot

Observation	Aurora Comments
Large impedance for decap C106	Vias connecting to C106 is too far

DC Voltage Drop Analysis

Source Setup and Result



Voltage Source

Component	Part	Source Voltage	Output Current
U2	xxx	3.3 V	2.0 A

Current Source

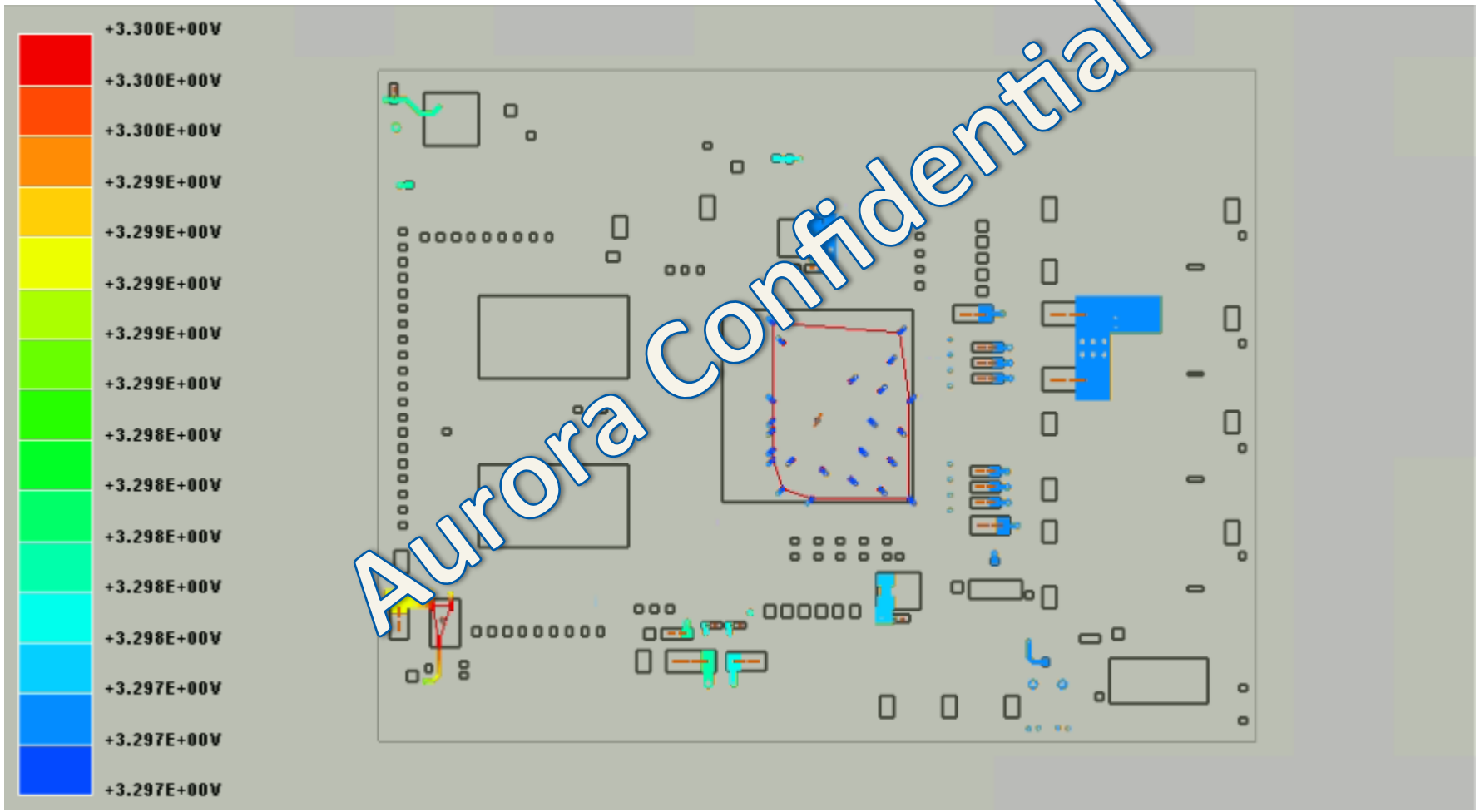
Component	Part	Source Current	Voltage Drop
U8	xxx	2.0 A	3.29569 V

Voltage Drop Summary

Net	Layer	Maximum (V)	Minimum (V)	Difference (mV)	Target
VCC_3V3	TOP	3.3	3.29714	13	99
VCC_3V3	POWER1	3.299055	3.297162	13	99
VCC_3V3	POWER2	3.297337	3.297188	13	99
VCC_3V3	BOTTOM	3.299055	3.297162	13	99
GND	TOP	1.45034e-3	0	1.5	10
GND	GND1	1.44151e-3	5.98055e-4	1.4	10
GND	GND2	1.43568e-3	8.08221e-4	1.4	10
GND	BOTTOM	1.43554e-3	8.19224e-4	1.4	10

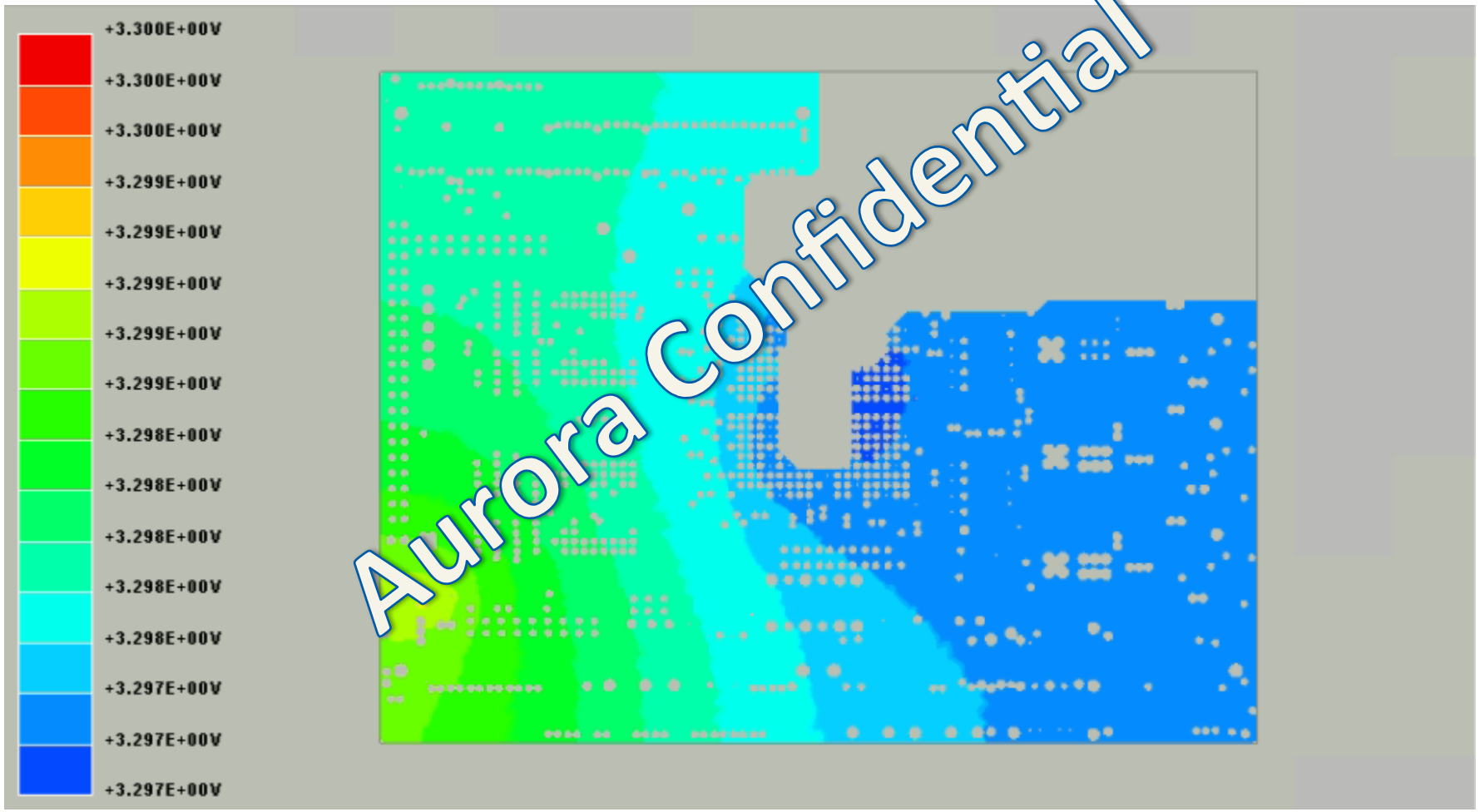
DC Voltage Distribution

Net: VCC_3V3 Layer: TOP



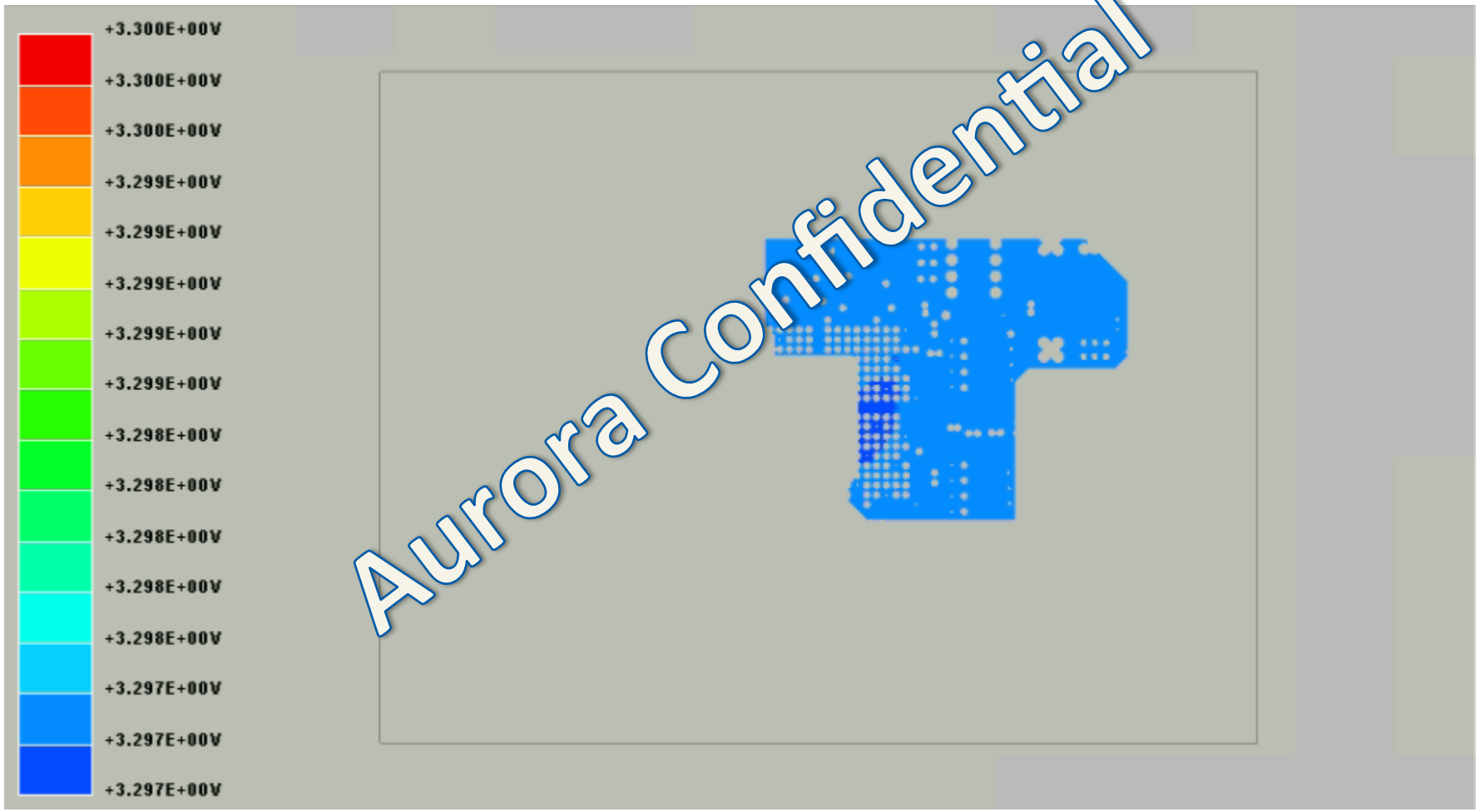
DC Voltage Distribution

Net: VCC_3V3 Layer: POWER1



DC Voltage Distribution

Net: VCC_3V3 Layer: POWER2

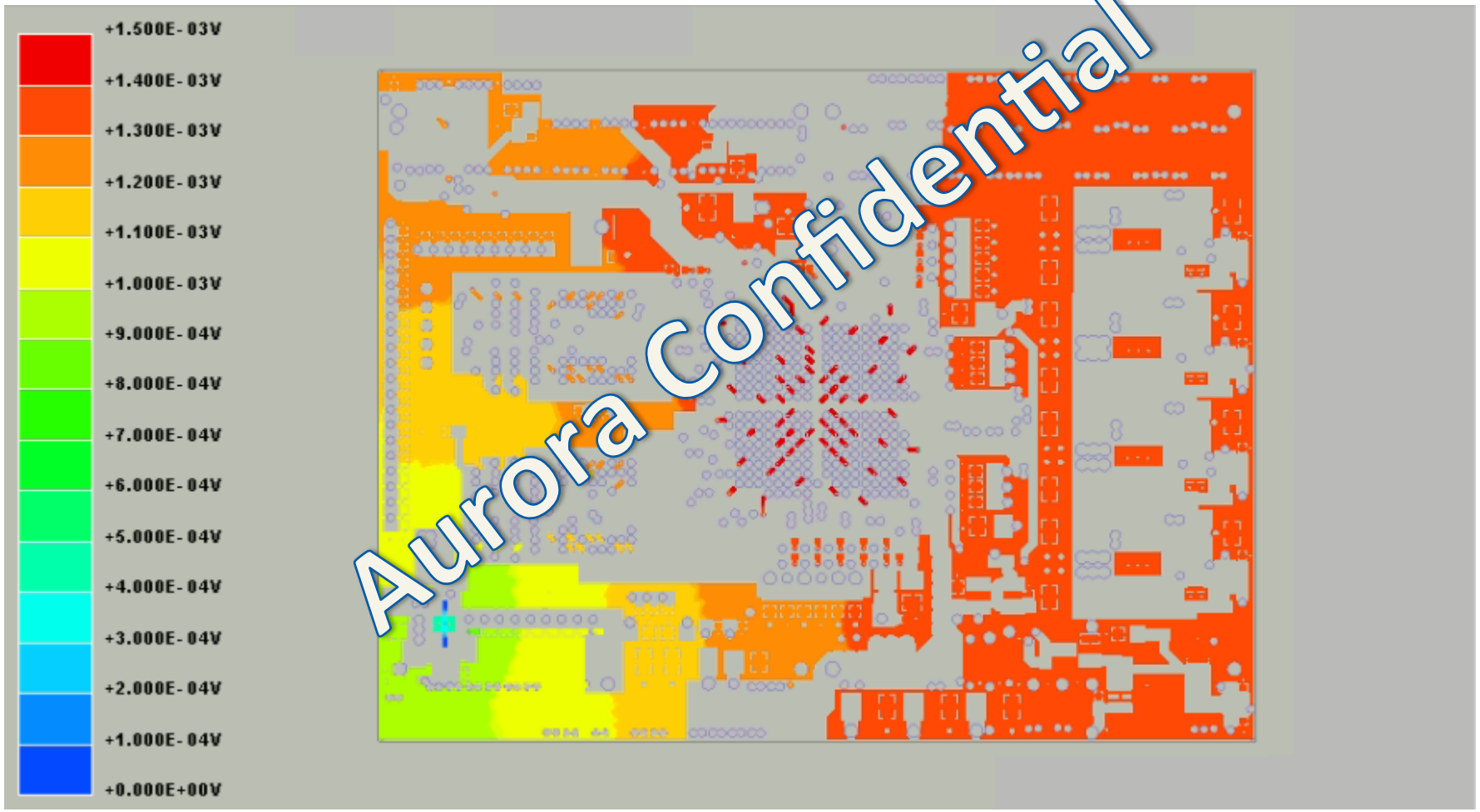


DC Voltage Distribution

Net: VCC_3V3 Layer: BOTTOM

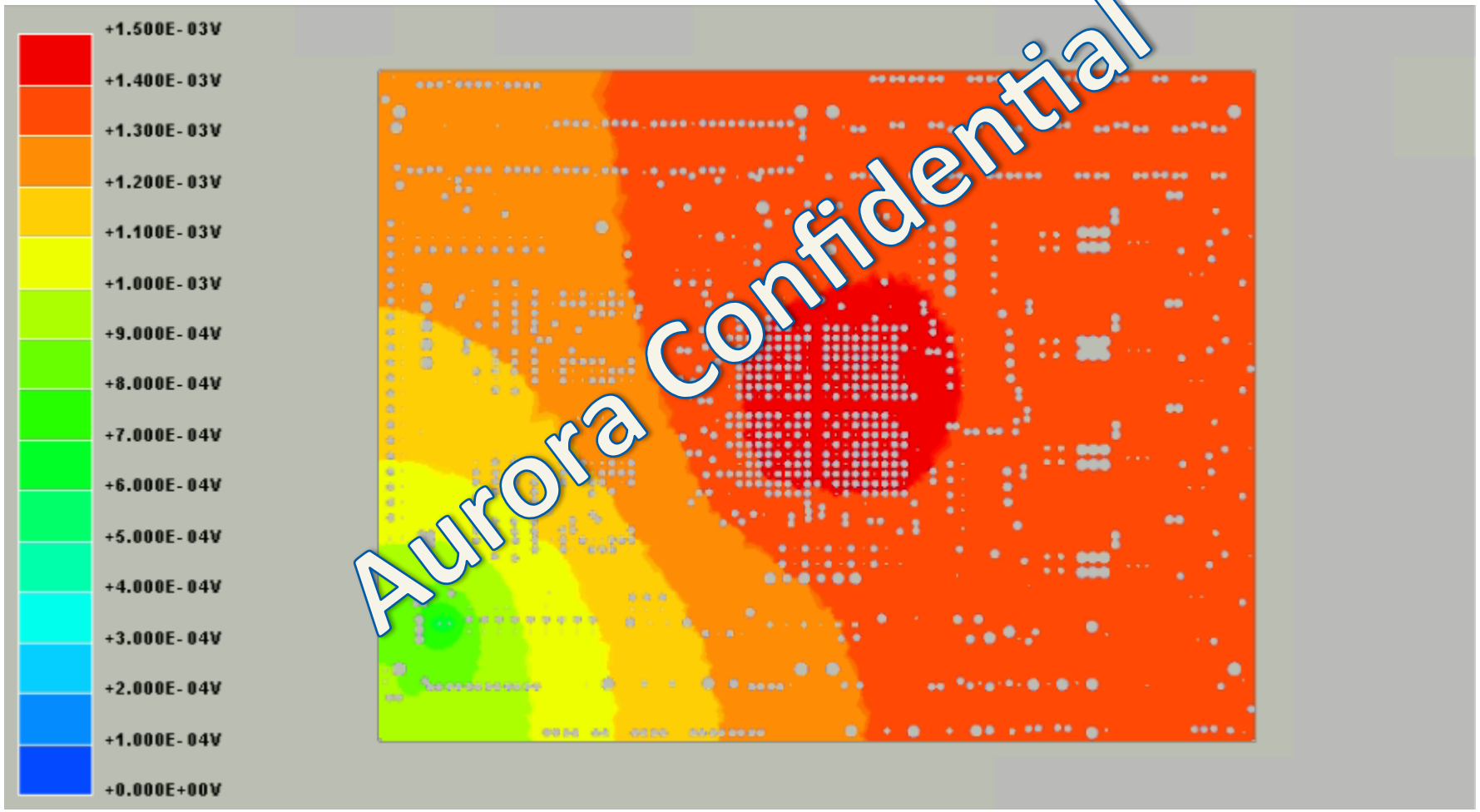
DC Voltage Distribution

Net: GND Layer: TOP



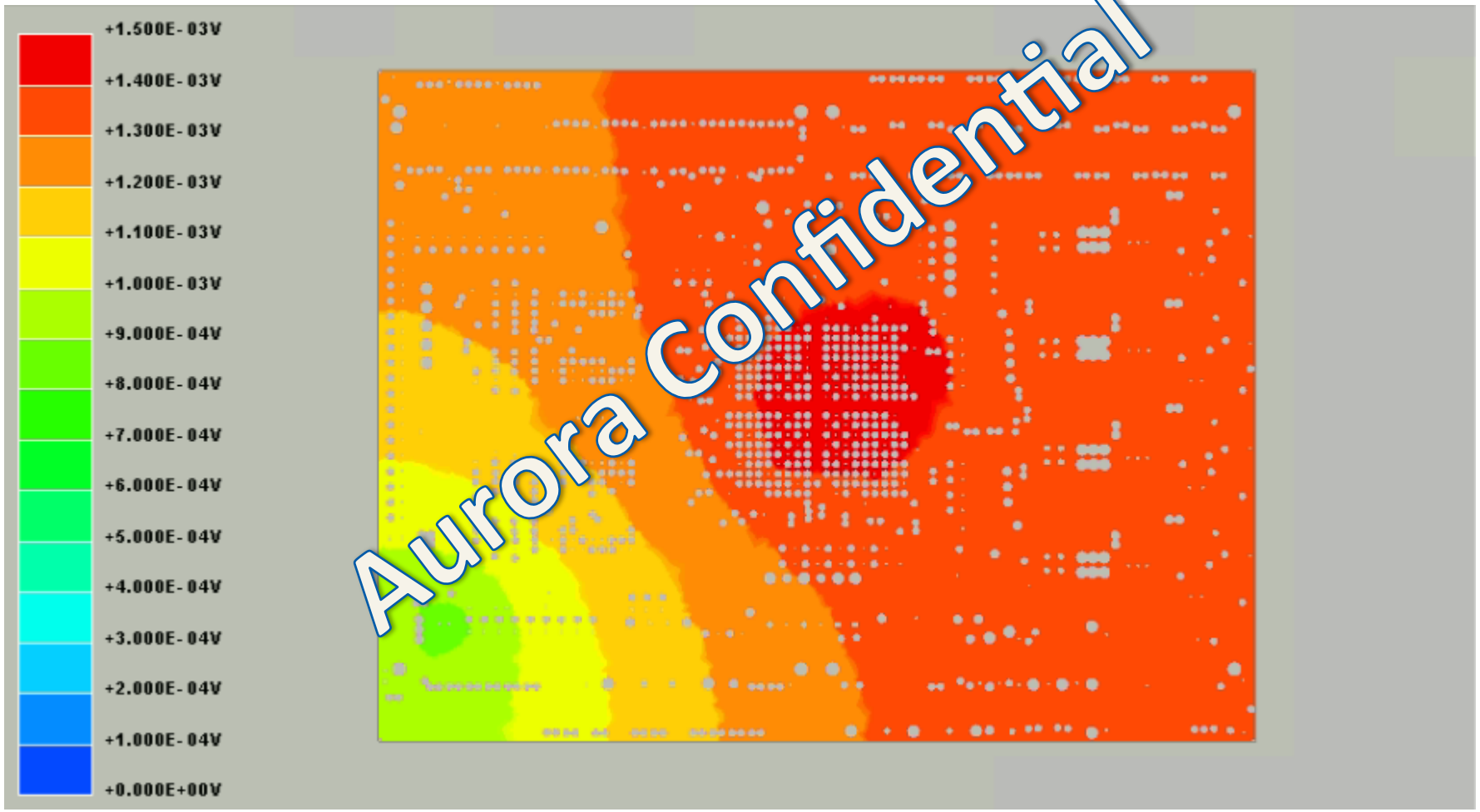
DC Voltage Distribution

Net: GND Layer: GND1



DC Voltage Distribution

Net: GND Layer: GND2



DC Voltage Distribution

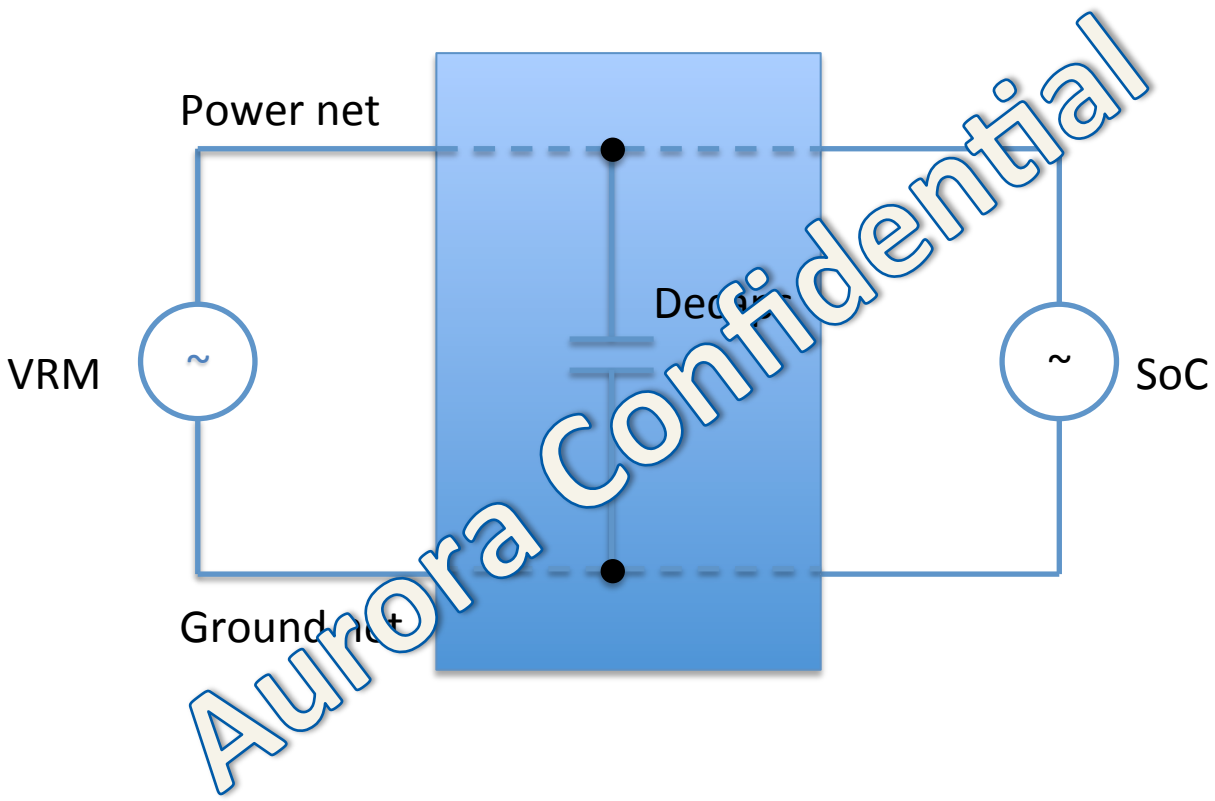
Net: GND Layer: BOTTOM

Maximum Via Current

Net	x (mm)	y (mm)	Current (A)	IR Drop (V)	Power (W)
VCC_3V3	-2.26E+01	-2.53E+01	5.12E-01	1.36E-04	6.95E-05
VCC_3V3	-2.26E+01	-2.53E+01	4.94E-01	1.31E-04	6.45E-05
VCC_3V3	-2.48E+01	-2.61E+01	4.89E-01	2.51E-04	1.23E-04
VCC_3V3	-2.48E+01	-2.53E+01	7.2E-01	9.86E-05	3.67E-05
VCC_3V3	-2.48E+01	-2.53E+01	3.54E-01	9.36E-05	3.31E-05
VCC_3V3	-2.55E+01	-2.64E+01	2.51E-01	1.29E-04	3.22E-05
VCC_3V3	-2.55E+01	-2.53E+01	2.49E-01	1.28E-04	3.17E-05
VCC_3V3	-2.[illegible]E+01	-3.24E+01	1.45E-01	7.46E-05	1.08E-05
GND	2.27E-01	-1.70E+01	1.28E-01	1.79E-05	2.29E-06
GND	-7.55E-01	-1.11E+01	9.31E-02	1.31E-05	1.22E-06

AC Impedance Analysis

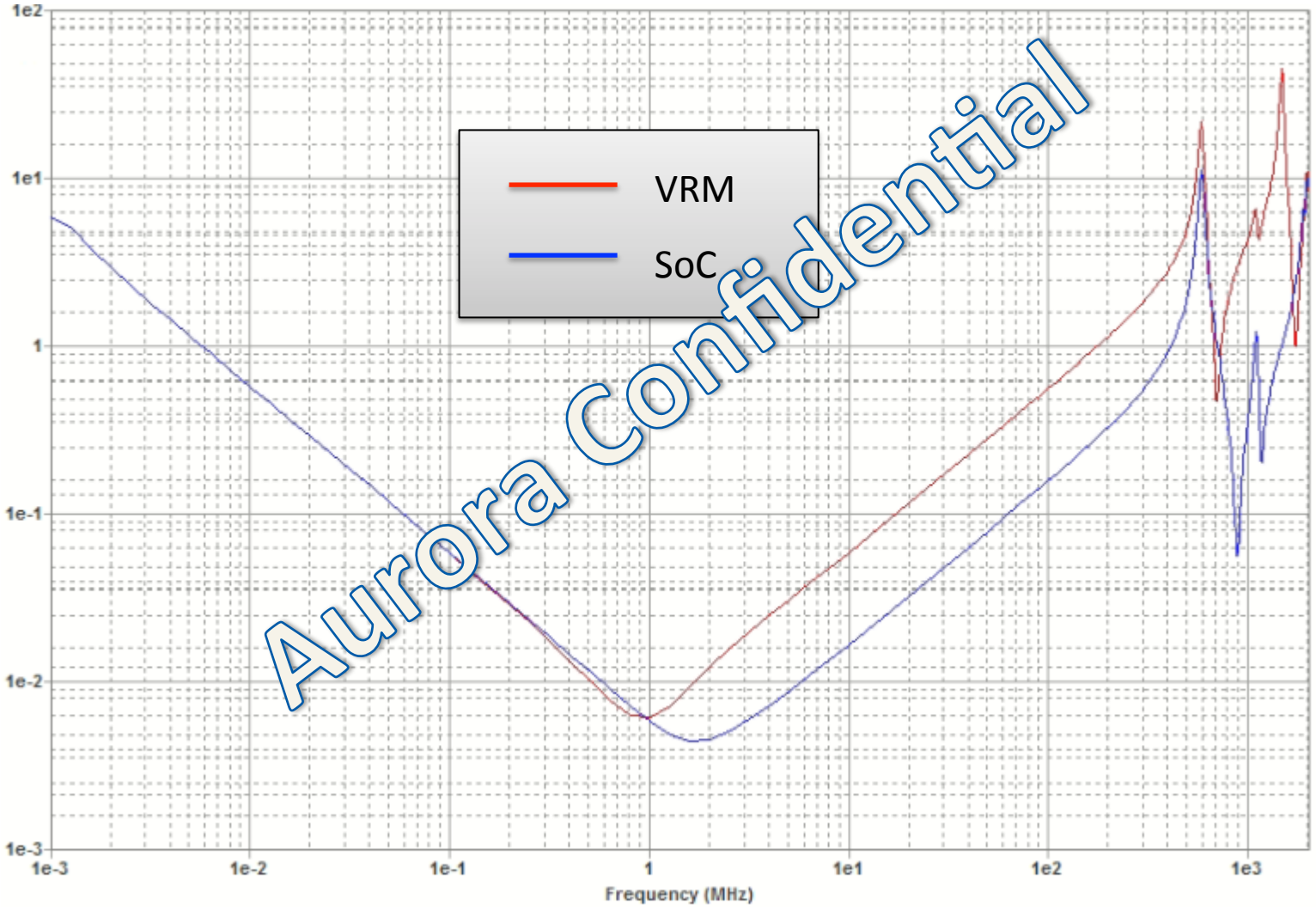
Analysis Setup



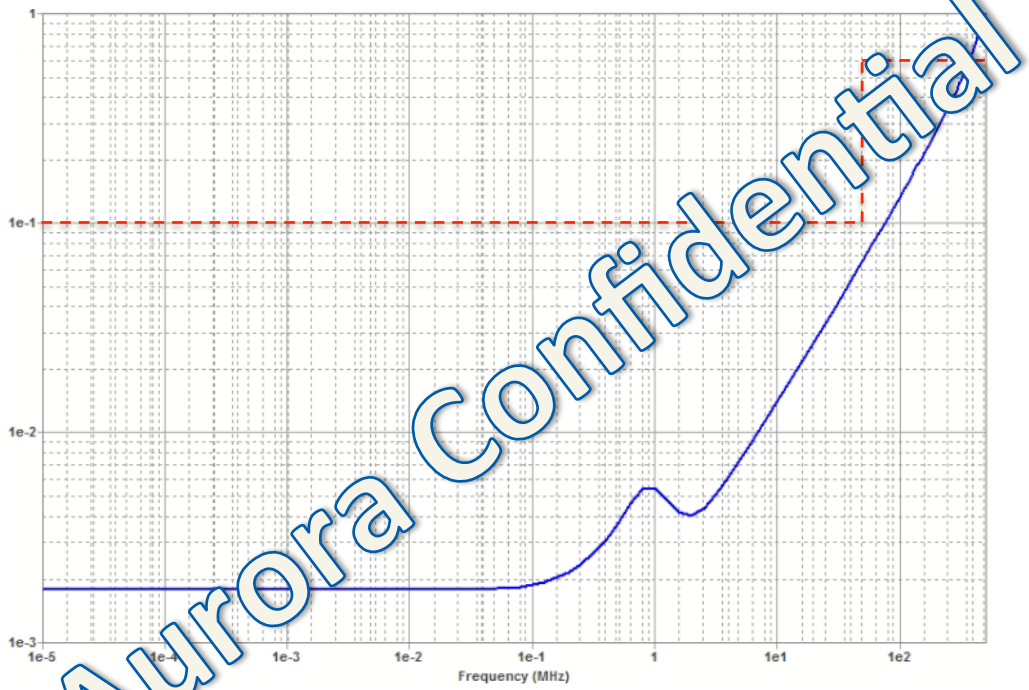
De-coupling Capacitors

Part	Components	Value	ESR (mOhm)	ESL (nH)
C0402_470NF	C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C165, C166	470 nF	25	0.2
C0603_4U7F	C107, C108, C109, C120, C121, C122, C164	4.7 uF	25	0.2
C0805_47UF	C105	47 uF	25	0.2
C0805_100UF	C106, C123	100 uF	25	0.2
C1206_47UF	C163	47 uF	25	0.2
C0402_100NF	C98, C95, C100, C104	100 nF	25	0.2
C0805_10UF	C5	10 uF	25	0.2
C1206_100UF	C36, C37	100 uF	25	0.2

Impedance Plot – VRM Open



SoC Input Impedance – VRM Short



Frequency	< 50 MHz (mΩ)	50 ~ 500 MHz (mΩ)
SPEC	100	600
Simulation	**67.1**	**1000**